R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 3-6, 12, 14, 15 and 17-21 under 35 U.S.C. §103 as being unpatentable over Hidaka et al. (U.S. Patent No. 4,730,320; hereinafter Hidaka) in view of Chen (U.S. Patent No. 4,464,753) has been obviated by appropriate amendment/is respectfully traversed and should be withdrawn.

The rejection of claims 2, 7-11, 13, and 16 under 35 U.S.C. §103 as being unpatentable over Hidaka in view of Chen in further view of Stiffler (U.S. Patent No. 4,736,376) has been obviated by appropriate amendment.

The rejection of claims 22 and 23 under 35 U.S.C. §103 as being unpatentable over Hidaka in view of Chen in further view of Stiffler (U.S. Patent No. 4,736,376) is respectfully traversed and should be withdrawn.

In contrast to the cited references, the presently claimed invention (claim 1) provides a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal and a bypass signal, where the bypass circuit comprises one or more logic gates configured to (i) receive the first syndrome signal at a first input, (ii) receive the bypass signal at a second input and (iii) present the second syndrome signal at an output. Claims 14 and 15 include similar limitations.

The cited references do not teach or suggest a bypass circuit as presently claimed. Therefore, the Office Action fails to meet the Office's burden of factually supporting a *prima facie* case of obviousness (MPEP §2142). As such, the present claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Specifically, assuming, *arguendo*, a person of ordinary skill in the art would consider the syndrome output circuit 70 in FIG. 6 of Hidaka to be similar to the presently claimed bypass circuit (as suggested on page 3, lines 7-17 of the Office Action and for which Applicants' representative does not necessarily agree), Hidaka does not teach or suggest a bypass circuit configured to generate a second syndrome signal in response to said first syndrome signal and a bypass signal, where the bypass circuit comprises one or more **logic gates configured to (i) receive the first syndrome signal at a first input, (ii) receive the bypass signal at a second input and (iii) present the second syndrome signal at an output**, as presently claimed. In particular, one of ordinary skill in the art would recognize the syndrome output circuit 70 of Hidaka as merely being pass transistors configured to direct the signal f of Hidaka to the syndrome decoder 6 of Hidaka or an output buffer 706 (see FIGS. 6 and 9 and column 6, line 44 through column 8, line 3 of Hidaka). A person of ordinary skill in the art would not view the pass transistors 704 and 705 in FIG. 9 of Hidaka as being the same as the presently claimed one or more

logic gates configured to (i) receive the first syndrome signal at a first input, (ii) receive the bypass signal at a second input and (iii) present the second syndrome signal at an output. Therefore, the cited references do not teach or suggest each and every element of the presently claimed invention as required to support a conclusion of obviousness (see MPEP §2142). As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-13 and 16-21 depend, directly or indirectly, from either claim 1 or claim 15 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

With respect to claim 22, the cited references do not teach or suggest each and every element of the present pending claim 22. Specifically, claim 22 provides a syndrome encoder circuit configured to generate a syndrome signal in response to a read data signal and a read parity signal, where the syndrome encoder circuit comprises a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

The position taken in the Office Action (see page 11, line 20 through page 12, line 6 of the Office Action) that "Figure 7 in Stiffler teaches first syndrome signal [c1...c4] is produced using non-inverting exclusive-Or gates and non-inverting exclusive-Or gates with an output inverted by a NOT gate is not technically correct. In particular, Stiffler does not support the interpretation presented in the Office Action. Specifically, Stiffler explicitly provides that the signals [c1...c4] are computed parity relationships which are used with nyble parity signals [g1...g4] **to generate syndrome bits.** Stiffler states:

> **Each circuit half combines the results of the four parity relationships computed from the data bits available to it with the four nyble parities computed by the other half circuit to generate four syndrome bits** (half of the total eight-bit syndrome). This combination is performed in second stage syndrome generators 442 and 444. Generator 442 receives **four bits, c1-c4, corresponding to the four computed parity relationships calculated from the input data bits** via bus 438 and **four nyble parities, g1-g4**, received from the other circuit half over terminal 441 and bus 440. Similarly generator 444 receives the complemented parity relationship bits, e1-e4, from generator 430 over bus 437 and the nyble parity bits g1-g4 from the other decoder half. Generator 442 generates four syndrome bits, h1-h4, on bus 456 and generator 444 generates four bits, i1-i4, which are the complements of the bits generated by generator 442. The complemented bits are provided on bus 454 to be used in a later stage of processing (column 8, line 63-column 9, line 13 of Stiffler, emphasis added).

Since the signals [c1...c4] are computed parity relationships rather than a syndrome signal, it follows that

Stiffler does not teach or suggest a syndrome encoder circuit configured to generate a syndrome signal in response to a read data signal and a read parity signal, wherein said syndrome encoder circuit comprises a type of syndrome encoder selected from the group consisting of (i) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (ii) inverting exclusive-OR gates, (iii) inverting exclusive-OR gates with an output inverted by a NOT gate, (iv) non-inverting exclusive-NOR gates, (v) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vi) inverting exclusive-NOR gates, and (vii) inverting exclusive-NOR gates with an output inverted by a NOT gate, as presently claimed. Therefore, Stiffler does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 23 depends directly from claim 22 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Robert M. Miller
Registration No. 42,892

Dated: July 29, 2005

c/o Peter Scott
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

Docket No.: 01-322 / 1496.00144